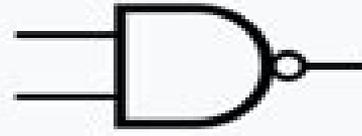


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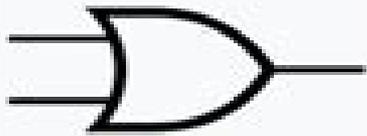
AND

Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1



NAND

Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0



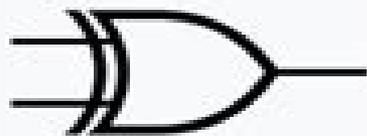
OR

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1



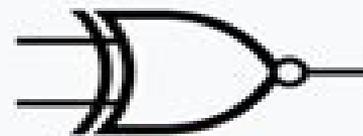
NOR

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	0



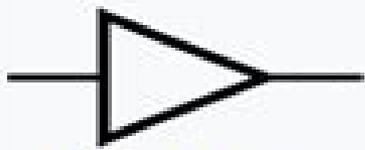
XOR

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	0



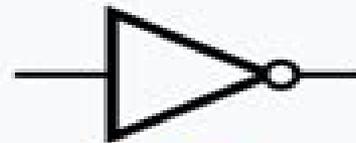
XNOR

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	1



Buffer

Input	Output
0	0
1	1



NOT

Input	Output
1	0
0	1

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William F. Leahy



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